CLAIMS

Please **AMEND** claims 36 and 41 as shown below.

The following is a complete list of all claims in this application.

1-13. (Cancelled)

14. (Previously Amended) A liquid crystal display, comprising:

a substrate;

a gate line assembly and a plurality of signal lines formed on the substrate, the gate line assembly comprising gate electrodes and gate lines;

a gate insulating layer covering the gate line assembly and the signal lines;

thin film transistor semiconductor patterns formed on the gate insulating layer;

a data line assembly comprising data lines crossing over the gate lines while being insulated from the gate lines, source electrodes extended from the data lines while contacting the semiconductor patterns, and drain electrodes contacting the semiconductor patterns in correspondence with the source electrodes;

a protective layer covering the data line assembly and the semiconductor patterns;

first contact holes exposing the drain electrodes;

second contact holes exposing the respective signal lines with a predetermined width, the second contact holes having a lateral side bordering on the signal line, the lateral side of the second contact holes having a length greater than the width of the second contact holes; and

pixel electrodes and subsidiary signal pads standing in the same plane, the pixel electrodes being connected to the drain electrodes, the subsidiary signal pads being connected to the signal lines.

15. (Original) The liquid crystal display of claim 14, wherein the gate line assembly and the signal lines have a double-layered structure with an aluminum-based layer.

16. (Original) The liquid crystal display of claim 15, wherein the second contact holes are formed at the gate insulating layer, the protective layer, and the aluminum-based layer of the signal lines.

17. (Original) The liquid crystal display of claim 14, further comprising a signal transmission film with signal leads, the signal leads connected to the signal lines in one to one correspondence.

18. (Previously Amended) The liquid crystal display of claim 17, wherein the signal leads of the signal transmission film comprise a first signal lead carrying high voltage signals and a second signal lead carrying low voltage signals, and a dummy lead is formed between the first signal lead and the second signal lead.

19. (Previously Amended) The liquid crystal display of claim 18, wherein a same voltage is applied to the dummy lead and the first signal lead.

20. (Original) The liquid crystal display of claim 18, wherein the dummy lead is several to several tens micrometers thick.

21. (Original) The liquid crystal display of claim 18, wherein a dummy line corresponding to the dummy lead is formed at the substrate.

22. (Original) The liquid crystal display of claim 21, wherein the dummy line is formed with a conductive material that is less oxidative than the signal line.

23. (Original) The liquid crystal display of claim 14, further comprising:

a gate pad connected to each gate line as a component of the gate line assembly;

a data pad connected to each data line as a component of the data line assembly;

a third contact hole exposing said gate pad with a predetermined width;

a fourth contact hole exposing said data pad with a predetermined width;

a subsidiary gate pad covering said gate pad at the third contact hole; and

a subsidiary data pad covering said data pad at the fourth contact hole.

24. (Original) The liquid crystal display of claim 23, wherein each of the third contact hole and the fourth contact hole has a lateral side bordering on the pad, the lateral side of the contact hole being longer than the width of the contact hole.

25. (Original) The liquid crystal display of claim 14, further comprising:

common voltage pads formed at the substrate, the common voltage pads being covered by one insulating layer among the gate insulating layer and the protective layer;

contact holes formed at the insulating layer with a predetermined width while exposing the common voltage pads, each contact hole having a lateral side bordering on the pad, the lateral side of the contact hole being longer than the width of the contact hole; and

subsidiary common voltage pads connected to the common voltage pads through the contact holes.

26. (Original) The liquid crystal display of claim 25, further comprising a color filter substrate with a common electrode, the common electrode being connected to the subsidiary common voltage pads.

27-35. (Cancelled).

36. (Currently Amended) A display device, comprising:

a first substrate having a plurality of gate lines and a plurality of data lines;

a plurality of thin film transistors electrically connected to the gate lines and the data lines;

a plurality of pixel electrodes electrically connected to the thin film transistors, respectively;

a plurality of gate driving ICs to output gate signals to the gate lines;

a plurality of data driving ICs to output data signals to the data lines;

a plurality of interconnection lines for applying gate control signals to at least one of the gate driving ICs; and

a black matrix overlapping at least one of the interconnection lines.

37. (Previously Added) The display device of claim 36, further comprising:

a second substrate sitting opposite the first substrate,

wherein the black matrix is formed on the second substrate.

38. (Previously Added) The display device of claim 36, further comprising:

a liquid crystal layer formed between the first substrate and the second substrate.

39. (Previously Added) The display device of claim 36, further comprising:

a driving signal transmission film,

wherein at least one of the data driving ICs is mounted on the driving signal transmission film.

40. (Previously Added) The display device of claim 39, wherein the driving signal transmission film outputs the gate control signals and the data signals to the interconnection lines and the data lines, respectively.

41. (Currently Amended) ~~The display of claim 36~~A display device, comprising:

a first substrate having a plurality of gate lines and a plurality of data lines;

a plurality of thin film transistors electrically connected to the gate lines and the data lines;

a plurality of pixel electrodes electrically connected to the thin film transistors, respectively;

a plurality of gate driving ICs to output gate signals to the gate lines;

a plurality of data driving ICs to output data signals to the data lines;

a plurality of interconnection lines for applyingapply gate control signals to at least one of the gate driving ICs; and

a black matrix overlapping at least one of the interconnection lines,

wherein one of the gate control signals is connected to at least one of the plurality of interconnection lines via a contact hole having a lateral side bordering the gate control signal and a length of the lateral side being longer than a width of the contact hole.